SEMICONDUCTOR DEVICE INCLUDING A RESISTIVE MEMORY LAYER AND METHOD OF MANUFACTURING THE SAME

CROSS-REFERENCES TO RELATED APPLICATION

[0001] The present application claims priority under 35 U.S.C. §119(a) to Korean application number 10-2015-0080657, filed on Jun. 8, 2015, in the Korean Intellectual Property Office, which is incorporated herein by reference in its entirety.

BACKGROUND

[0002] 1. Technical Field

[0003] Various embodiments generally relate to a semiconductor device and a method of manufacturing the same and, more particularly, to a semiconductor device including a resistive memory layer and a method of manufacturing the semiconductor device.

[0004] 2. Related Art

[0005] Increasing semiconductor device integration requires maximizing the number of memory cells in a limited amount of substrate area. One method of accomplishing this is constructing vertical transistors having vertical channels. Variable resistive memory devices having resistive memory layers use vertical transistors as access elements. The resistive memory layer is located over the vertical transistors.

[0006] Operational characteristics of memory cells in a variable resistive memory device are dependent on memory cell dimensions. Thus, memory cell uniformity, and especially resistive memory layer uniformity, is required to produce high quality memory devices.

SUMMARY

[0007] According to exemplary embodiments, there is provided a method of manufacturing a semiconductor device. The method may include: sequentially forming an interfacial conductive layer and an etch stop layer on a resistive memory layer; forming a main conductive layer on the etch stop layer; exposing a portion of the etch stop layer by patterning the main conductive layer; exposing a portion of the interfacial conductive layer by patterning the portion of the etch stop layer; forming an upper electrode structure by patterning the portion of the interfacial conductive layer; cleaning a surface of the upper electrode structure and an exposed surface of the resistive memory layer; and patterning the resistive memory layer using the upper electrode structure as an etch mask.

[0008] According to exemplary embodiments, there is provided a method of manufacturing a semiconductor device. The method may include: forming a resistive memory layer on a lower electrode; forming a barrier layer, which includes an interfacial conductive layer and an etch stop layer, on the resistive memory layer; forming a conductive layer on the barrier layer; forming an upper electrode by patterning the conductive layer until the etch stop layer is exposed; forming an etch stop layer pattern by patterning the etch stop layer using the upper electrode as an etch mask; forming a barrier layer pattern including an interfacial conductive layer pattern and an etch stop layer pattern by removing an exposed portion of the interfacial conductive layer; and forming a resistive memory layer pattern by etching the resistive memory layer using the upper electrode and the barrier layer pattern as etch masks. At that time, a conductive adhesive layer may be further interposed between the carbon layer and the main conductive layer.

[0009] According to exemplary embodiments, there is provided a semiconductor device. The semiconductor device may include a lower electrode, a resistive memory layer and an upper electrode. The resistive memory layer may be formed on the lower electrode. The upper electrode may be formed on the resistive memory layer. The upper electrode may include a conductive layer, a carbon layer and a main conductive layer sequentially stacked.

[0010] According to exemplary embodiments, there may be provided a semiconductor device. The semiconductor device may include a lower electrode, a resistive memory layer, an upper electrode and a barrier layer. The resistive memory layer may be formed on the lower electrode. The upper electrode may be formed on the resistive memory layer. The barrier layer may be interposed between the resistive memory layer and the upper electrode. The barrier layer may include a first: conductive layer, a carbon layer and a second conductive layer.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] Exemplary embodiments can be understood in more detail from the following detailed description taken in conjunction with the accompanying drawings. FIGS. **1** to **19** represent non-limiting, exemplary embodiments as described herein.

[0012] FIGS. **1** to **12** are cross-sectional views illustrating a method of manufacturing a semiconductor device in accordance with exemplary embodiments;

[0013] FIG. **13** is a cross-sectional view illustrating a semiconductor device including a resistive memory layer in accordance with exemplary embodiments;

[0014] FIGS. **14** and **15** are perspective views illustrating a semiconductor device including a resistive memory layer in accordance with exemplary embodiments;

[0015] FIG. **16** is a cross-sectional view illustrating a semiconductor device including a resistive memory layer in accordance with exemplary embodiments;

[0016] FIG. **17** is a block diagram illustrating a microprocessor in accordance with exemplary embodiments;

[0017] FIG. **18** is a block diagram illustrating a processor in accordance with exemplary embodiments; and

[0018] FIG. **19** is a block diagram illustrating a system in accordance with exemplary embodiments.

DETAILED DESCRIPTION

[0019] Various exemplary embodiments will be described more fully hereinafter with reference to the accompanying drawings, in which some exemplary embodiments are shown. The present invention may, however, be embodied in many different forms and should not be construed as limited to the exemplary embodiments set forth herein. Rather, these exemplary embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the present invention to those skilled in the art. In the drawings, the sizes and relative sizes of parts and thicknesses of layers may be exaggerated for clarity.

[0020] It will be understood that when an element or layer is referred to as being "on," "connected to" or "coupled to"